

WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising the steps of:
 - forming a resist pattern over a base layer;
 - applying a resist pattern smoothing material onto a surface of the resist pattern, thereafter heating and developing the resist pattern applied with the resist pattern smoothing material so as to form a smoothed resist pattern; and
 - etching the base layer using the smoothed resist pattern as a mask so as to form a pattern of the base layer,
 - wherein at least one of an application thickness of the resist pattern smoothing material and a heat temperature for the heating is adjusted so as to smooth at least wall surfaces of the resist pattern.
2. A method of manufacturing a semiconductor device according to Claim 1, wherein a maximum opening dimension D_{max} (nm) and a minimum opening dimension D_{min} (nm) of the smoothed resist pattern are within a range of ±5% with respect to a predetermined opening dimension D (nm) of the resist pattern.
3. A method of manufacturing a semiconductor device according to Claim 1, wherein a maximum opening dimension D_{max} (nm) and a minimum opening dimension D_{min} (nm) of the smoothed resist pattern are within a range of ± 3% with respect to a predetermined

opening dimension D (nm) of the resist pattern.

4. A method of manufacturing a semiconductor device according to Claim 1, wherein a predetermined opening dimension D (nm) of the resist pattern, and an average opening dimension Dav. (nm) of the smoothed resist pattern whose wall surfaces have been smoothed satisfy the relation expressed by:

$$\text{Dav. (nm)} \geq \text{D (nm)} \times (90/100).$$

5. A method of manufacturing a semiconductor device according to Claim 1, wherein a predetermined opening dimension D (nm) of the resist pattern, and an average opening dimension Dav. (nm) of the smoothed resist pattern whose wall surfaces have been smoothed satisfy the relation expressed by:

$$\text{Dav. (nm)} \geq \text{D (nm)} \times (95/100).$$

6. A method of manufacturing a semiconductor device according to Claim 1, wherein the resist pattern is formed of an ArF resist.

7. A method of manufacturing a semiconductor device according to Claim 1, wherein an opening dimension D (nm) of the smoothed resist pattern is within a range of 50 nm to 150 nm.

8. A method of manufacturing a semiconductor device according to Claim 1, wherein the heat temperature is within a range of 80 °C to

100 °C.

9. A method of manufacturing a semiconductor device according to Claim 1, wherein the application thickness of the resist pattern smoothing material is within a range of 70 nm to 100 nm.
10. A method of manufacturing a semiconductor device according to Claim 1, wherein the resist pattern smoothing material comprises a resin, a crosslinking agent, and a surfactant.
11. A method of manufacturing a semiconductor device according to Claim 10, wherein the resist pattern smoothing material has one of water-solubility and alkali-solubility.
12. A method of manufacturing a semiconductor device according to Claim 10, wherein the surfactant is a non-ionic surfactant.
13. A method of manufacturing a semiconductor device according to Claim 12, wherein the non-ionic surfactant is at least one of polyoxyethylene - polyoxypropylene condensation compound, polyoxyalkylene alkylether compound, polyoxyethylene alkylether compound, polyoxyethylene derivative compound, sorbitan fatty acid ester compound, glycerin fatty acid ester compound, primary alcohol ethoxylate compound, phenol ethoxylate compound, alkoxylate compound, fatty acid ester compound, amide compound, alcohol

compound, and ethylene diamine compound.

14. A method of manufacturing a semiconductor device according to Claim 10, wherein the resin is at least one of polyvinyl alcohol, polyvinyl acetal, and polyvinyl acetate.

15. A method of manufacturing a semiconductor device according to Claim 10, wherein the crosslinking agent is at least one of melamine derivative, urea derivative, and uril derivative.

16. A method of manufacturing a semiconductor device according to Claim 10, wherein the resist pattern smoothing material further comprises one of a water-soluble aromatic compound and a resin having an aromatic compound in a portion thereof.

17. A method of manufacturing a semiconductor device according to Claim 16, wherein the water-soluble aromatic compound is one of polyphenol compound, aromatic carboxylic acid compound, naphthalene polyhydric alcohol compound, benzophenone compound, flavonoid compound, derivatives thereof and glycosides thereof, and the resin containing an aromatic compound in a portion thereof is one of polyvinyl aryl acetal resin, polyvinyl aryl ether resin, and polyvinyl aryl ester resin.

18. A method of manufacturing a semiconductor device according to

Claim 10, wherein the resist pattern smoothing material further comprises an organic solvent.

19. A method of manufacturing a semiconductor device according to Claim 18, wherein the organic solvent is at least one of alcohol solvent, chain ester solvent, cyclic ester solvent, ketone solvent, chain ether solvent, and cyclic ether solvent.

20. A method of forming a resist pattern comprising the step of:
 applying a resist pattern smoothing material onto a surface of the resist pattern, thereafter heating and developing the resist pattern applied with the resist pattern smoothing material,
 wherein at least one of an application thickness of the resist pattern smoothing material and a heat temperature for the heating is adjusted so as to smooth at least wall surfaces of the resist pattern.